On page 1, line 11, please change "[1]" to --DIN 25424, Part 1: Fehlerbaumanalyse: Methode und Bildzeichen; Part 2: Handrechenverfahren zur Auswertung eines Fehlerebaums--.

On page 1, line 12, please change "[2]" to --J. Dekleer and B. C. Williams, Diagnosing Multiple Faults, , Elsevier Science Publishers, Artificial Intelligence, Vol. 32, 1987, pp. 97-130--.

On page 1, line 20, please change "[2]" to --the Dekleer et al reference--.

On page 1, line 24, please change "[2]" to --the Dekleer et al reference--.

On page 2, line 12, please change "[3]" to --K. Nökel, K. Winkelmann, Controller Synthesis and Verification: A Case Study, in: C. Leverentz, T. Lindner, Formal Development of Reactive Systems, Lecture Notes in Computer Science (No. 891), Springer 1995, pp. 55-74--.

On page 2, line 18, please change "[4]" to --J. Burch et al, Symbolic Model Checking for Sequential Circuit Verification, IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems, Vol. 13, No. 4, pp. 401-424, April 1994--.

On page 2, line 21, please change "[5]" to --R. Bryant, Symbolic Boolean Manipulation with Ordered Binary-Decision Diagrams, ACM Computing Survey, Vol. 24, No. 3, pp. 293-318, September 1992--.

On page 2, after line 23, as a separate line before line 24, please insert the following heading:

--**SUMMARY OF THE INVENTION**--.

On page 2, please delete lines 27-28.

On page 2, line 29, after "method" please insert --according to the present invention--.

On page 3, please delete lines 22-23.

On page 4, please delete lines 15-17 and insert the following heading and paragraph:

--**BRIEF DESCRIPTION OF THE DRAWINGS**

The features of the present invention which are believed to be novel, are set forth with particularity in the appended claims. The invention, together with further objects and advantages, may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in the several Figures of which like reference numerals identify like elements, and in which:--.

On page 4:

line 18, after "Figure 1" please insert --is--;

line 19, after "Figure 2" please insert --is--;

line 23, after "Figure 3" please insert --is--;

line 26, after "Figure 4" please insert --is--;

line 28, after "Figure 5" please insert --is--.

On page 5:

line 1, after "Figure 6" please insert --is--;

line 3, after "Figure 7" please insert --is--;

line 5, after "Figure 8" please insert --is--;

line 6, after "Figure 9" please insert --is--.

On page 5, after line 7, as a separate line before line 8, please insert the following heading:

--**DESCRIPTION OF THE PREFERRED EMBODIMENTS**--.

On page 7, line 17, please change "[4]" to --J. Burch et al, Symbolic Model Checking for Sequential Circuit Verification, IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems, Vol. 13, No. 4,

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pp. 401-424, April 1994--.

On page 11, line 30, please change "implement" to --use--.

On page 12, line 13, please change "[5]" to --R. Bryant, Symbolic Boolean Manipulation with Ordered Binary-Decision Diagrams, ACM Computing Survey, Vol. 24, No. 3, pp. 293-318, September 1992--.

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On page 15, line 13, please change "in error [...]" to --for the occurrence of error--.

On page 15, line 14, please change "[1]" to --DIN 25424, Part 1: Fehlerbaumanalyse: Methode und Bildzeichen; Part 2: Handrechenverfahren zur Auswertung eines Fehlerebaums--.

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On page 15, after line 18, please insert the following paragraph:

--The invention is not limited to the particular details of the method and apparatus depicted and other modifications and applications are contemplated. Certain other changes may be made in the above described method and apparatus without departing from the true spirit and scope of the invention herein involved. It is intended, therefore, that the subject matter in the above depiction shall be interpreted as illustrative and not in a limiting sense.--.

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IN THE CLAIMS:

On page 16, line 1, please change "**PATENT CLAIMS**" to --**WHAT IS CLAIMED IS:**--